501.42869X00



IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Applicants:

H. CHAKIHARA, et al.

Application No.:

10/629,733

Filed:

July 30, 2003

For:

A SEMICONDUCTOR MEMORY DEVICE AND A METHOD OF

MANUFACTURING THE SAME, A METHOD OF

MANUFACTURING A VERTICAL MISFET AND A VERTICAL

MISFET, AND A METHOD OF MANUFACTURING A SEMICONDUCTOR DEVICE AND A SEMICONDUCTOR

DEVICE

Art Unit:

2826

Examiner:

F. Abraham

UNDER 37 CFR §§ 1.97 & 1.98

Commissioner for Patents P.O. Box 1450 Alexandria, VA 22313-1450 December 30, 2004

Sir:

In the matter of the above-identified application, applicants are submitting herewith copies of the documents listed in the attached form PTO/SB/08A for the Examiner's consideration.

This Information Disclosure Statement is being submitted before the mailing date of either a final action or a notice of allowance and is accompanied by the fee of \$180.00 set forth in 37 CFR '1.17(p).

Each of the documents listed on the attached form PTO/SB/08A is in the English language.

It is respectfully requested that this Information Disclosure Statement be considered by the Examiner.

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Application No.: 10/629,733 Docket No.: 501.42869X00

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Respectfully submitted,

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Approved for use through 10/31/2002. OMB 0651-0031

U.S. Patent and Trademark Office: U.S. DEPARTMENT OF COMMERCE

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Complete if Known Substitute for form 1449A/PTO **Application Number** 10/629,733 INFORMATION DISCLOSURE Filing Date July 30, 2003 STATEMENT BY APPLICANT First Named Inventor H. CHAKIHARA, et al Art Unit 2826 (use as many sheets as necessary) Examiner Name F. Abraham Sheet 1 of 1 **Attorney Docket Number** 501.42869X00

U.S. PATENT DOCUMENTS						
Examiner Initials'	Cite No.1	Document Number Number-Kind Code ² (if known)	Publication Date MM-DD-YYYY	Name of Patentee or Applicant of Cited Document	Pages, Columns, Lines, Where Relevant Passages or Relevan Figures Appear	
-		6,740.921	05-2004	Matsuoka et al.		
				 		
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FOREIGN PATENT DOCUMENTS						
Examiner Initials'	Cite No. ¹	Foreign Patent Document	Publication Date	Name of Patentee or Applicant of Cited Document	Pages, Columns, Lines,	T ⁶
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OTHER PRIOR ART—NON PATENT LITERATURE DOCUMENTS				
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		H. Takato, et al., "High Performance CMOS Surrounding Gate Transistor (SGT) for Ultra High Density LSIs", 1988 IEEE, pp 222-225		

Examiner	Date		
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